WHAT IS CLAIMED IS:

1. A multi-bank testing apparatus for a synchronous DRAM consisting of a plurality of banks, comprising:

a row address strobe generating unit for enabling a word line to transmit data from cells to bit line sense amplifiers in each bank of said synchronous DRAM;

a column address strobe generating unit for generating a signal adapted to enable transistors respectively adapted to couple bit lines carrying data, amplified by said bit line sense amplifiers, to local data bus lines;

input/output sense amplifiers for amplifying data on said local data bus lines, respectively;

a transmission gate unit for controlling transmission of data from said input/output sense amplifiers to global read data bus lines; and

an input/output comparing unit for compressing data from said input/output sense amplifiers prior to said transmission thereof to said global read data bus lines.

2. The multi-bank testing apparatus as claimed in claim 1, wherein said row address strobe generating unit comprises:

a first PMOS transistor and a first NMOS transistor connected in series to each other, said first PMOS and NMOS transistors receiving a row address strobe signal in a common fashion at gates thereof;

a timing controller coupled to a node between said first PMOS and NMOS transistors and adapted to control the period of time for which an output from said row address strobe generating unit;

a group of second NMOS transistors coupled in series together and connected in series to said first NMOS transistor, each of said

second NMOS transistors receiving an associated one of bank selection address signals at a gate thereof;

a third NMOS transistor coupled to a node between said first NMOS transistor and said second NMOS transistor group in a fashion parallel to said second NMOS transistor group, said third NMOS transistor receiving, at a gate thereof, an all-bank test signal being enabled when write and read operations in a test mode are to be conducted for all banks.

3. The multi-bank testing apparatus as claimed in claim 1, wherein said column address strobe generating unit comprises:

a first PMOS transistor and a first NMOS transistor connected in series to each other, said first PMOS and NMOS transistors receiving a column address strobe signal in a common fashion at gates thereof;

a timing controller coupled to a node between said first PMOS and NMOS transistors and adapted to control the period of time for which an output from said column address strobe generating unit;

a group of second NMOS transistors coupled in series together and connected in series to said first NMOS transistor, each of said second NMOS transistors receiving an associated one of bank selection address signals at a gate thereof;

a third NMOS transistor coupled to a node between said first NMOS transistor and said second NMOS transistor group in a fashion parallel to said second NMOS transistor group, said third NMOS transistor receiving, at a gate thereof, an all-bank test signal being enabled when write and read operations in a test mode are to be conducted for all banks.

4. The multi-bank testing apparatus as claimed in claim 1, wherein said transmission gate unit comprises:

a plurality of first transmission gates each arranged between an output of an associated one of said input/output sense amplifiers and an associated one of said global read data bus lines, each of said first transmission gates being closed in response to an all-bank test signal being enabled when write and read operations in a test mode are to be conducted for all banks, thereby preventing data from said associated input/output sense amplifier from being transmitted to said associated global read data bus line; and

a pair of second transmission gates each arranged between an output of said input/output comparing unit and an associated one of said input/output global read data bus lines, each of said second transmission gates being opened by said all-bank test signal, thereby allowing said output from said input/output comparing unit to be transmitted to said associated global read data bus line.

5. The multi-bank testing apparatus as claimed in claim 4, wherein:

each of said first transmission gate comprises

a first PMOS transistor and a first NMOS transistor coupled in parallel between said associated input/output sense amplifier and a first one of two global read data bus lines respectively associated with input and input-bar signals from said input/output sense amplifier, said first PMOS transistor receiving, at a gate thereof, said all-bank test signal while said first PMOS transistor receiving, at a gate thereof, a signal inverted from said all-bank test signal via an inverter, and

a second PMOS transistor and a second NMOS transistor coupled in parallel between said associated input/output sense amplifier and a second one of said associated global read data bus lines, said second PMOS transistor receiving, at a gate thereof, said all-bank test signal while said second NMOS

transistor receiving, at a gate thereof, a signal inverted from said all-bank test signal via said inverter; and each of said second transmission gates comprises

a third PMOS transistor and a third NMOS transistor coupled in parallel between said input/output comparing unit and said first associated global read data bus line, said third PMOS transistor receiving, at a gate thereof, said signal inverted from said all-bank test signal via said inverter while said third NMOS transistor receiving, at a gate thereof, said all-bank test signal, and

a fourth PMOS transistor and a fourth NMOS transistor coupled in parallel between said input/output comparing unit and said second associated global read data bus line, said fourth PMOS transistor receiving, at a gate thereof, said signal inverted from said all-bank test signal via said inverter whereas said fourth NMOS transistor receiving, at a gate thereof, said all-bank test signal.

6. The multi-bank testing apparatus as claimed in claim 1, wherein said input/output comparing unit comprises:

a pair of first PMOS transistors and a pair of first NMOS transistors coupled together in parallel and adapted to receive, at respective gates thereof, a signal inverted by an inverter from an all-bank test signal being enabled when write and read operations in a test mode are to be conducted for all banks;

a plurality of second PMOS transistors coupled in parallel between one of said first PMOS transistors and one of said first NMOS transistors and adapted to receive, at respective gates thereof, input signals;

a second NMOS transistor coupled to one of said first NMOS transistors in such a fashion that they have a common source;

a plurality of third PMOS transistors coupled in parallel between the other one of said first PMOS transistors and the other one of said first NMOS transistors and adapted to receive, at respective gates thereof, input-bar signals;

a third NMOS transistor connected to other one of said first NMOS transistors in such a fashion that they have a common source;

a first NAND gate adapted to receive said input and input-bar signals;

a second NAND gate adapted to receive an output from said first NAND gate at one input thereof, said second NAND gate also receiving said all-bank test signal at the other input thereof; and

a third NAND gate adapted to receive an output from said second NAND gate via inverters at one input thereof, said third NAND gate also receiving an output from said second NAND gate via said inverters and then via other inverters, said third NAND gate being coupled at an output thereof to gates of said second and third NMOS transistors in a common fashion via an inverter.

7. The multi-bank testing apparatus as claimed in claim 6, wherein said input and input-bar signals are those output from said input/output sense amplifiers transmitted to the same global read data bus line and enabled in response to the same column address.

8. The multi-bank testing apparatus as claimed in claim 6, wherein said input and input-bar signals are those output from said input/output sense amplifiers associated with the same bank and enabled in response to the same column address.